



Smart Transformer for Enhanced Efficiency and
Sustainability in Maritime Transportation

Deliverable D2.2 – Report MVDC/LVDC SST

Eaton Industries GmbH

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Abstract

Deliverable abstract	
The deliverable D 2.2 presents the report on the MVDC/LVDC converter for the solid-state transformer, are submitted in three parts in the months M8, M24 and M33 of the project. The first submission mainly presents the design concept of the MVDC/LVDC converter including technical requirements, electrical specifications, topology selection and simulation overview. D 2.2 is aligned with the task T 2.5: Development of high-power density 1 MW MVDC/LVDC SST converter under the work package 2 of project STEESMAT.	

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1 Introduction

The STEESMAT project aims to demonstrate technologies and methodologies that will enable the deployment and system integration of onboard DC grids for large vessels. To this extent, a power distribution system based on medium voltage DC (MVDC) and low voltage DC (LVDC) is proposed in the project as shown in the Figure 1. Further details on the power distribution system are described in detail in the deliverable D4.1: System definition and characterisation report. The solid-state transformer (SST) consisting of the power conversion stages MVAC/LVDC conversion and MVDC/LVDC conversion constitutes the central part of the DC grid. Further, isolated and non-isolated DC/DC converters are connected to the fuel cell and battery packs in the low voltage DC grid. This report focuses on the MVDC/LVDC converter coupling the 5 kV DC grid with the 800 V low voltage DC grid.

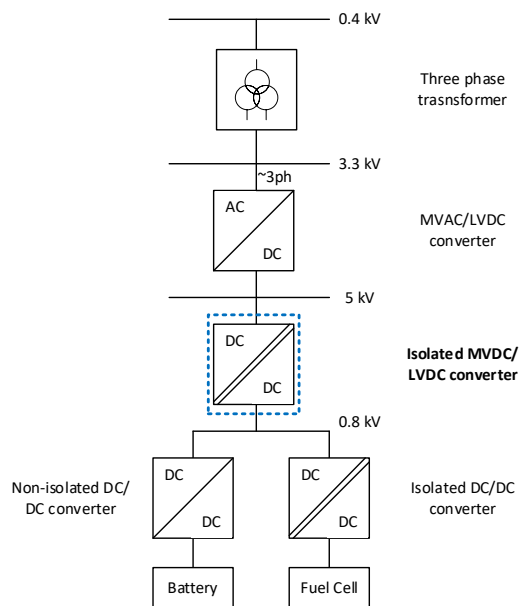


Figure 1: Schematic diagram of the proposed power distribution system

2 Technical requirements

The technical requirements for the MVDC/LVDC are addressed in different domain such as electrical specifications, environment and mechanical requirements, control and protection, and safety and classification. Relevant standards applicable to the onboard power distribution system deployment for each of these domains are taken into consideration. For e.g., the input medium voltage imposes isolation requirements on the individual modules or power electronic building blocks (PEBB) and on the cabinet assembly of the MVDC/LVDC converter. The parameters considered are basic and reinforced insulation, clearance and creepage distances, pollution degree, protection impedance and thermal and mechanical safety. Relevant standards for e.g., IEC 62477-2:2018 [1] and IEEE Std 1709-2018 [2] are considered for the development. More details on requirements are provided in the next submission of the D2.2.

3 Electrical Specifications

Based on the power distribution system, the main electrical specifications of the MVDC/LVDC converter were identified and are summarized in the table.

Table 1: Electrical specifications

Parameter	Value
Input voltage	5000 V
Output voltage	800 V
Maximum power	Up to 1 MW
Controllers	Separate MV and LV side
Power semiconductors	1.2 kV devices
Cooling method	Forced air cooled

4 Topology selection

The suitable topologies for the MVDC/LVDC converter based on the electrical specifications are the input series and output parallel (ISOP), Modular multilevel converter (MMC) applicable to DC/DC power conversion [3] and quadruple active bridge (QAB) topology [4] for the configuration of the PEBBs. A single unit is highlighted in each of the configurations.

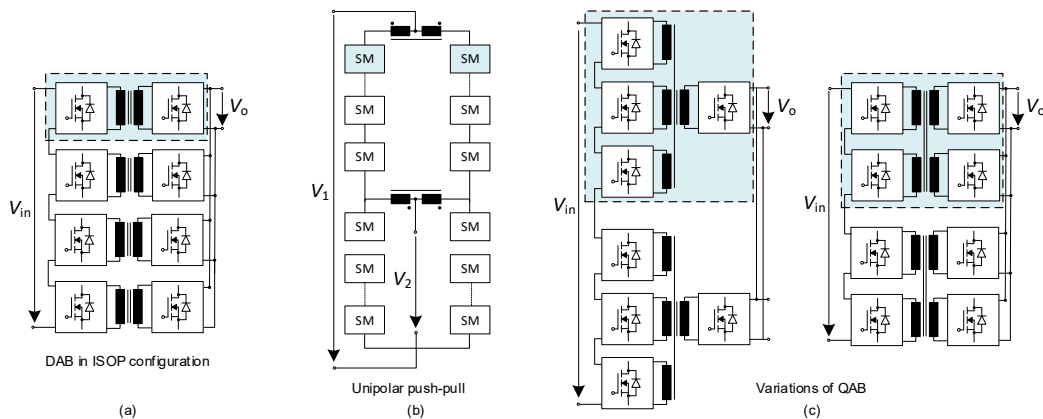


Figure 2: Topologies for configuration of the power electronic building blocks a) ISOP, b) MMC and c) QAB

The comparison between the topologies is shown in Table 2. Due to reasons such as high input voltage scalability, low control complexity and high redundancy, the ISOP topology is selected for this application.

Table 2: Topology comparison for the MVDC/LVDC converter

	ISOP	MMC	QAB
Input configuration	Series	Series	Series
Output configuration	Parallel	Series	Parallel
Output voltage scalability	Limited	High	Limited
Output current scalability	High	Limited	High
Voltage balancing complexity	Input	Input/Output	Input
Redundancy	High	Low	Low to moderate
Control complexity	Low	Moderate to high	High
Magnetics Design complexity	Low	Medium	High

The MVDC/LVDC converter consist of several active and passive components. Among the active components, the power semiconductors are the crucial. The input voltage of 5 kV requires either power semiconductors with high voltage blocking capability > 5 kV, or a cascaded approach is necessary, reducing the requirements on the blocking voltage capability of the power semiconductors. IGBTs are available in the market that can be used in non-cascaded configuration, but this would demand low switching frequency (< 1 kHz), resulting in larger size of the magnetics and passive components in the DC/DC converter. In STEESMAT, along with efficiency the emphasis is also on the power density. Therefore, the SiC power semiconductors based on wide bandgap technology are considered.

SiC power semiconductors from different manufacturers having breakdown voltages from 1.2 kV up to 3.3 kV were considered for the topology. Although with the 3.3 kV devices the number of cells can be reduced, the high ON resistance, high switching losses and low switching frequency make such devices unattractive for the MVDC/LVDC converter. Based on the superior electrical characteristics and the commercial maturity, 1.2 kV SiC devices are selected.

5 Simulation

Within the task T2.5: Development of high-power density 1MW MVDC/LVDC SST converter, the simulations of the MVDC/LVDC converter will be performed. The simulation outcomes regarding each PEBB from the task T 2.4: Development of power electronics building blocks for MVDC/LVDC converter are taken in consideration for simulating the complete MVDC/LVDC converter. An overview of the control architecture is provided in the Figure 3.

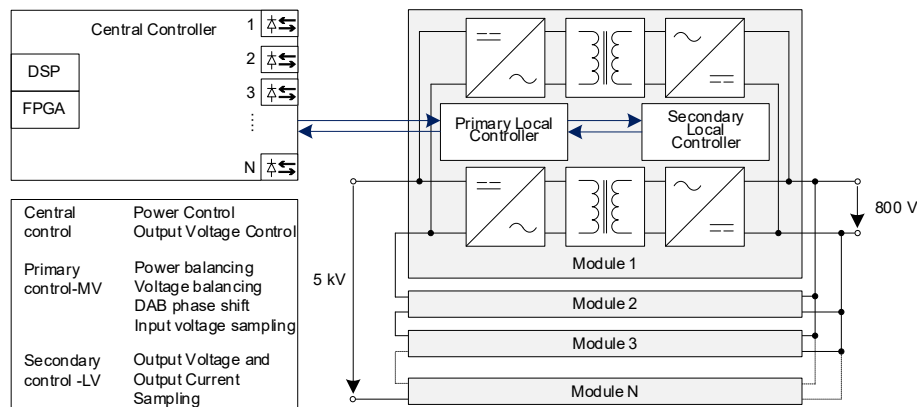


Figure 3: Control architecture of the MVDC/LVDC converter [5] (modified)

The modules are connected in series on the medium voltage side and in parallel on the low voltage side. Each module consists of MV cell, LV cell and a medium frequency transformer. Each cell on the MV or LV side has a local controller which is controlled by the central controller. The MV controller has the tasks like the power balancing, voltage balancing whereas the central controller controls the output power of the complete MVDC/LVDC converter. LV cell controller provides the output current and voltage signals to the MV cell controller. The simulation objectives are summarized in the Figure 4. Upon validation of the simulations, passive and active components for the MVDC/LVDC converter will be selected. Details on the controller hardware design, control algorithms and controller testing and validation are provided in the next part of the D2.2.

5.1 Electrical performance

This includes the simulation for the soft switching analysis of the power semiconductors at different operating conditions of load and output voltage of the MVDC/LVDC converter. The efficiency of the converter will be simulated over partial and full load. The output voltage regulation is simulated with the modules in ISOP configuration considering step response analysis, and the output voltage ripple.

5.2 Control strategy

Several tasks will be performed for the verification of the control strategy of the MVDC/LVDC converter. It is crucial that the input voltage is distributed among each module, active voltage balancing is necessary to avoid unequal stressing of the power semiconductors. On the output side, current sharing between the modules is mandatory for equal loading of the modules. Since the control architecture is based on local and central controllers, synchronization between modules is simulated. Other tasks such as fault detection, pre-charging of the DC capacitors and bidirectional power transfer capability of the converter will be simulated in the T2.5: Development of high-power density 1MW MVDC/LVDC SST converter.

5.3 Thermal analysis

Thermal simulations of the modules in the MVDC/LVDC converter are performed for e.g., thermal loading of the cells in case of asymmetry in voltage and current balancing are analysed. Temperature rise under overload conditions are simulated for the power semiconductor modules and magnetics.

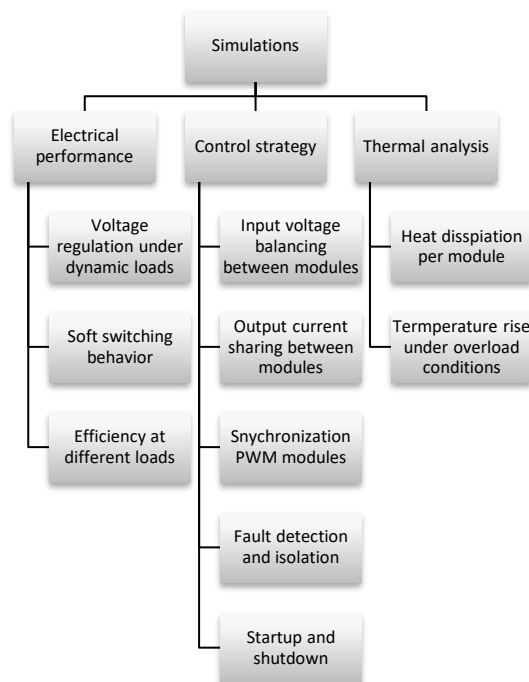


Figure 4: Simulation objectives under the task T2.5 - Development of high-power density 1MW MVDC/LVDC SST converter

Along with the above objectives, inputs will be provided for the converter control assessment on the hardware in the loop (HiL) platforms. Converter control models will be imported in the HiL simulations and tested within the task T2.7: HiL real time simulation of SST converters.

6 References

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